IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Terry R. Lee

Application No.: 09/583,883

Group Art Unit: 2189

Filed: May 31, 2000

Examiner: Kim T. Huynh

For: HIGH SPEED BUS TOPOLOGY FOR EXPANDABLE SYSTEMS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION OF TERRY R. LEE UNDER 37 CFR 1.131

Dear Sir:

I, Terry R. Lee, declare and state as follows:

1. I reside at 17 Evergreen Drive, Boise, Idaho 83716.

2. I am the inventor of the subject matter described and claimed in the above-identified U.S. patent application ("the '883 application"), filed on May 31, 2000, as evidenced by the attached the executed Declaration document (Exhibit A).

3. I have reviewed and understand the '883 application, including the currently pending claims and amendments (the "Claimed Invention").

4. I conceived the invention covered by the Claimed Invention prior to May 10, 2000, as evidenced by Exhibit B, which is a Micron Invention Disclosure document. The actual date on this submission has been blanked out, as has any description not relevant to the conception of the Claimed Invention; however, the date of the Invention Disclosure is prior to May 10, 2000. Micron Technology Inc. is the assignee of the present application as evidenced by Exhibit C.

5. The law firm of Dickstein Shapiro Morin & Oshinsky LLP ("Dickstein") was assigned to write this application, as evidenced by attached Exhibit D, which is a copy of a letter from Dickstein to Micron, forwarding a first draft of the patent application, identified by reference number M4065.0260/P260, for my review. The actual date on this submission has been blanked out, as has any description not relevant to the conception of the Claimed Invention; however, the date is prior to May 10, 2000. I received this draft and provided comments to the attorney through an e-mail to Micron's legal department, as evidenced by Exhibit E, which is a printout of email correspondence between myself, Micron and a Dickstein Attorney. Dates prior to May 10, 2000 have been blanked out.

6. Following the Exhibit E correspondence Dickstein prepared and forwarded to the Micron legal department a final signature draft of the patent application as evidenced by Exhibit F. The actual date on this submission has been blanked out, as has any

description not relevant to the conception of the Claimed Invention; however, the date is prior to May 10, 2000.

7. The signature draft of the application covering the Claimed Invention was forwarded to me by the Micron legal department. After reviewing the signature draft of the application covering the Claimed Invention, I approved the filing of the application. My approval was sent to the Micron legal department in an e-mail dated May 26, 2000 as evidenced by Exhibit G (information not relevant to the conception of the Claimed Invention has been blanked out). The Micron legal department forwarded my e-mail to Dickstein on May 30, 2000 (Exhibit G). The present application was filed in the United States Patent and Trademark Office on May 31, 2000. The preparation of the presentation of the present application covering the Claimed Invention was diligently pursued from prior to the reference date of May 10, 2000 to the date of filing (May 31, 2000) of the present application.

8. The present application covering the Claimed Invention and the Assignment and Declaration documents were executed after the present application was filed (see Exhibits A and C).

All statements made herein of my own knowledge are true and all statements made on information and belief are believed to be true; and these statements were made

with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the above-identified patent.

Date: August 21, 2003 By: Terry R. Lee

Terry R. Lee

94-1184

Micron Technology, Inc.

Invention Disclosure

RECEIVED
[redacted]

If this disclosure is related to an ARPA project, please check one of the following:

☐ Advanced SRAM ☐ BST ☐ FED ☐ FE RAM ☐ NCAICM

1) **INVENTOR(s):** Terry R. Lee

Not Employed by Micron:

2) **DESCRIPTION:**

2.1 Title of Invention:
High Speed Bus Topology for Expandable Systems

2.2 Brief Description of Invention:
See attached.

2.3 Attach a complete description, including drawings or sketches and articles relevant to the invention. Legible photocopies of laboratory notebooks are acceptable.

3) **INFORMATION CONCERNING CONCEPTION OF INVENTION:**

3.1 Conception and Documentation of the Invention:

a. Identify the date when you first conceived the invention.
(If not sure, give the earliest date of which you are sure)
See attached.

b. To whom was the idea first described and on what date?
(Other than co-inventor)
See attached.

c. Identify the date of the first tangible record such as computer simulation, tape out, drawing, or written description. Please type and location.
See attached.

[redacted]

3.2 Conception of the Invention:

a. Identify any related invention disclosures, patents, or other publications describing similar .ideas, and other companies working in the same field. Attach copies if available.

b. What is the closest technology, of which you are aware?
the Rambus RIMM module

c. Identify the advantages of this invention over previous technology.
See attached

3.3 Important Dates:

a. Has the invention been disclosed outside the company ☐ YES ☒ NO
If yes, to whom, when, and in what form was the invention disclosed?

b. Have any articles describing your invention been published? ☐ YES ☒ NO
If yes, list author(s), title of the article, name of publication, and date?

c. Have any engineering samples been given out? ☐ YES ☐ NO
If yes, to whom and on what date?

d. Has any product using the invention been sold or offered for sale?
☐ YES ☐ NO If yes, to whom and on what date?

3.4 Disposition of the Invention:

a. When will (or did) Micron begin use of the invention experimentally?

b. When will (or did) Micron begin production of this invention?

3.5 Miscellaneous Information:

a. Was the invention developed during a joint development agreement or other contract with an outside company? ☐ YES ☐ NO

b. Please list developmental work outside of the company (including government proposal or contract)

[redacted]

4) **INVENTOR(S):**

Name: Terry R. Lee

Micron Phone: 368-3819 Mail Stop: 607

Department: DRAM Allocable Dept #: 430I

PLEAS

Company Name (***Very Important***):

- [X] Micron Technology, Inc.
- [ ] Micron Communications, Inc.
- [ ] Micron Quantum Devices, Inc.
- [ ] Other

Home Address: 17 Evergreen Dr.
Boise, ID 83716

Citizenship: US

Supervisor: Jeff Mailloux

Signature: Terry R. Lee Date: [redacted]

(all inventors must sign and date this disclosure form before it can be accepted)

Name:

Micron Phone: Mail Stop:

Department: Dept #:

Company (Very Important):

- [ ] Micron Technology, Inc.
- [ ] Micron Communications, Inc.
- [ ] Micron Quantum Devices, Inc.
- [ ] Other

Home Address:

Citizenship:

Supervisor:

Signature: _____ Date: _____

(all inventors must sign and date this disclosure form before it can be accepted)

KLL

Name:

Micron Phone: Mail Stop:

Department: Dept #:

Company (Very Important):

- ☐ Micron Technology, Inc.
- ☐ Micron Communications, Inc.
- ☐ Micron Quantum Devices, Inc.
- ☐ Other

Home Address:

Citizenship:

Supervisor:

Signature: _____ Date: _____

(all inventors must sign and date this disclosure form before it can be accepted)

(for additional inventors copy the previous the page)

5) **WITNESS:**

If there is only one inventor, a witness should sign and date this disclosure. A witness in this case is a non-inventor who understands the nature of the invention.

Signature: _____ Date: [redacted]

Note: If you have any questions or you need assistance completing this form, please call the Patent Department, ext. 84520.

paloyd

From: monicak
Sent: [redacted]
To: paloyd
Subject: FW: Patent Disclosure for High Speed Bus Topology

-----Original Message-----
From: kryan
Sent: [redacted]
To: monicak
Cc: mikelynch
Subject: RE: Patent Disclosure for High Speed Bus Topology

I confirm that I have read and do understand this invention.

-----Original Message-----
From: tlee
Sent: [redacted]
To: monicak
Cc: kryan; mikelynch
Subject: Patent Disclosure for High Speed Bus Topology
Importance: High

Monica,

Attached is a patent disclosure for a high-speed bus topology. I was not able to download a patent disclosure form prior to leaving town, so I filled in all the details that I recall that the regular disclosure form asks for. I also am not able to log into the Merc. We need to file this disclosure as quickly as possible, since I will need to share this information with other companies. Mike Lynch is aware of this situation. I intend to present this on Saturday in Tokyo, so we would like to get as much progress as feasible by that time. I would like to follow up and file as soon as possible, to prevent others from filing that concept after we share the information.

In the disclosure, I refer to Figures 1-4. The figures are included in the attached presentation (pdf file), and they are in order, but not numbered. The presentation may also be useful for the patent attorney. If an attorney wishes to contact me, it will be necessary to leave questions via voicemail or email, since it will be difficult for me to have a phone conversation until I return next week.

By sending this email, I agree to all of the assignments and to the accuracy of the disclosure that is called out in our regular disclosure form. Please accept this email as a proxy to my signature, until I can sign the document when I return to Boise. Kevin Ryan will witness the invention, so please accept his proxy by reply, or arrange to have him sign the document. Thanks for your help with this.

Terry

<< File: ModuleBus.doc >> << File: Techmtg2_bus.PDF >>

[redacted]

[redacted]

[redacted]CEIVED

[redacted]

Title: High Speed Bus Topology for Expandable Systems

Inventor: Terry R. Lee

Employee Number: 4778

Co-Inventors: None

Department: DRAM Components Allocable, 4301
Supervisor: Jeff Mailloux

Invention First Conceived: [redacted]

This has not yet been used in any Micron product

The first product that this would be considered for is a high speed DRAM module that could go into production in 2002

This has not yet been disclosed outside of Micron to any competitors or customers.

First evidence of the invention is a presentation that was created on [redacted]. The material will be presented on [redacted] to a small group of companies under a non-disclosure agreement. The expected attendees are NEC, Hyundai, Infineon, Samsung, and Intel.

This invention has been witnessed by Kevin Ryan.

The closest technology that I am aware of to this invention is the Rambus RIMM module.

Background of the invention:

A variety of computing or networking platforms require the ability to expand the hardware over time to improve the performance of this system, or to accommodate new users. Expansion capabilities are typically provided for graphics cards, input/output cards, network cards, microprocessors, SRAM, and DRAM. These expansion cards are typically integrated on a printed circuit board (PCB) that can easily be inserted or removed by the user. Typically, the PCB is insert into a connector and provide an electrical attachment to a bus.

The expandable bus is typically on a host PCB, often called a motherboard. Connectors are mounted on the motherboard to provide slots for hardware expansion. The bus connects to the add-in card through the connector. This connection typically results in a connection stub up to the receiving component on the add-in card. The stubs are electrically undesirable for high-speed busses, since they provide a discontinuity of impedance along the bus which results in reflected energy on to the bus.

Some of the techniques that have been used to reduce the effect of the stubs on the bus include the use of series resistors on the add-in cards. This technique isolates the stubs from the main bus, and the resistors help to dissipate the energy of the reflected waves traveling up and down the stub. The resistor technique has the disadvantage of inserting a voltage drop on a driven signal, which requires a larger supply voltage for the device output drivers. Another technique loops the bus through the add-in card and back out the same connector. With this technique, a card, or extender card, must be populate every connector slot in order to maintain a continuous bus. This technique reduces the stub length of the connector since the bus travels in and out of the card, rather than adding a stub to the bus. One disadvantage of this approach is that the bus becomes very long. In the case of an add-in memory card, approximately six inches of bus is added for every slot. The longer bus has disadvantages for high-speed systems, since the propagation delay (flight time) is longer to get from one end of the bus to the other, and the bus has less bandwidth than a shorter bus due to parasitic capacitance and inductance, and due to attenuation in the PCB.

What is needed is a high-speed bus system that allows replaceable and expandable cards that provides better bandwidth than the existing systems.

[redacted]

Brief Description of the Invention:

This invention describes a modified high-speed bus topology for use in expandable or replaceable card systems, such as network switches and computers. This invention increases the maximum operating bandwidth of the bus, since the bus is relatively short without stubs and reflections. The bus maintains a uniform transmission line impedance by looping into the card on one connector and out of the card on another connector. The use of a second connector, instead of looping out on the same connector, results in a shorter bus, since the connector can be located at a distance that is less than the width of the card. This is particularly beneficial in memory DIMM cards, since the card width is typically 5.25 inches, but the card height is only 1.25 inches. In this case, the second connection can be provided with an edge connector on the top of the card, and a bus jumper is used to provide an electrical connection from the top of one DIMM to the top of an adjacent DIMM. In a high-speed system it would be desirable to design this jumper with a controlled transmission line impedance.

Description of the Invention:

A conventional high-speed bus system that is can be used in network switches, network hubs, or computing systems is shown in Figure 1. For the purpose of this description, the focus will be on a main memory subsystem for a computer; however, the same technique is appropriate for any high-speed bus that has removable cards. The cards insert into a connector for attachment to the bus. The device on the left will typically be a memory controller that is physically located on the computer motherboard. Two slots are shown for increasing the memory storage capacity, but this invention applies to multiple slots where the number of slots is determined by the maximum bus operating frequency, or by the maximum desired memory capacity. In the computer main memory example, the connectors can be 184-pin DIMM connectors with DDR SDRAM DIMM modules.

Referring to Figure 1, a resistor is typically included at either or both ends of the bus for high-speed signal termination. The resistor value is normally chosen to be equal to the loaded characteristic impedance of the transmission line system, so there will be no wave reflections resulting from a mismatch in impedance at the end of the bus. A typical resistor value is 25 to 28 ohms, although other values are possible.

In the system shown, series (stub) resistors are included on the memory DIMMs near the interface to the connector. The series resistor serves two purposes for improving the signal integrity and increasing the bandwidth of the bus system. First, the resistors help to increase the impedance of the stub, and thereby, isolate the stub better from the main motherboard bus. Second, the resistor helps to attenuate the reflected energy that travels up and down the module stub from the motherboard to the main memory bus. The technique is quite effective for reducing reflections and improving the operating bandwidth, but it also has some drawbacks. There is some added system cost and module layout complexity associated with the large number of resistors. In the DDR SDRAM DIMM, the data bus width can be 64 or 72 bits, for example. Since there is termination at the end of the bus, there becomes a DC path for current from the DRAM driving the bus, through the stub resistor, and into the parallel resistor to a termination voltage (typically referred to as VTT). The series resistor reduces the voltage swing of the signal on the bus, so it is either necessary to reduce the driver impedance, or to increase the output driver supply voltage, VDDQ, on the DRAM. Reducing the drive impedance requires a larger device, and this will increase the input/output capacitance of the DRAM. This higher capacitance has the effect of reducing bus bandwidth, so a larger VDDQ voltage is typically used.

Figure 2 shows an alternative bus topology that loops the bus through the memory module, instead of providing stub style connection to the devices on the module. Eliminating the stubs is effective in improving the operating bandwidth, provided that a uniform transmission line impedance is maintain throughout all sections of the bus. This requires that the connector impedance match the bus trace impedance, and that the section of the module that the DRAMs are located have the same loaded characteristic impedance as the sections without devices. A typical motherboard PCB line impedance will be around 60 ohms for a minimum width line. However, in the section where the DRAM devices are located, there is an increase in capacitance per unit length due to the DRAM input capacitance, and therefore, the effective impedance is reduced. In the populated section of the module, a loaded impedance of 25 to 30 ohms is typical. In order to achieve a uniform bus impedance, it is necessary to increase the line widths of the bus in the unpopulated sections so that its impedance is equal to the impedance of the populated sections. This layout restriction becomes impractical for larger bus widths due to the congestion of the bus in areas

on the board, and due to the amount of board surface area that the bus uses. Further, the lower bus impedance requires a lower termination resistance, and this dissipates more power for a given signal swing.

Another disadvantage of the bus topology in Figure 2, is that the bus length gets very long. The longer bus length results in an increase in propagation delay from when the controller drives the bus until the information is received at the DRAM. This is referred to as flight time. The longer flight time increases the latency from when the controller requests information until the information is received at the controller, and the increased latency reduces computer system performance. Longer flight times can also reduce the efficiency of the bus for moving information. Typically there is a brief waiting period that occurs between one device releasing the bus and a different device driving the bus. This waiting period is necessary to allow the data to propagate to one end of the bus and/or to allow the bus voltage to settle to a stable state. In the case of a DRAM driving the bus followed by the controller driving the bus, the controller must wait until the previous data is received at the controller before the controller turns on its driver, otherwise the data will be corrupted.

A similar waiting period can occur when one DRAM releases the bus before another DRAM drives the bus. If there is already a voltage waveform propagating on the bus, this can result in excessively high or low voltages on the bus when the second DRAM drives the bus. Since it isn't practical for the bus to maintain a perfectly uniform impedance, there will be some reflected energy also travelling up and down the bus. If the bus voltage is not in a stable state when the next DRAM drives the bus, it will effect the transition time of the signal moving through the reference voltage. This will result in an increase or decrease in delay of the recognition of a logical zero or one voltage, and this delay change results in timing uncertainty, or timing errors which can corrupt the data that is latched into the receiving device. This is a form of intersymbol interference where a previous data value can effect the capture of the next data bit or symbol.

Another disadvantage of the longer bus is a reduction in maximum operating bandwidth. Since the bus is not physically ideal, there is attenuation and dielectric leakage in the PCB. These losses result in a reduction of signal swing, and the losses get worse at higher frequencies. Since there is also reflected energy travelling up and down the bus, there becomes a limit as to how high of data rate that can be effectively transmitted on the bus.

Still another disadvantage of a long bus is that in can increase the electomangetic interference (EMI) of the system. EMI increases as the cross-sectional area of a signal and its ground return path are increased. In the example, a signal transmitted from the controller will travel down the bus, and its electromagnetic wave return path will predominately be along the ground plane located under the signal. In a PC system, the memory modules are typically 5.25 inches wide by 1.25 inches tall, so the bus length through the module is over six inches. For a three module system, the total bus length can be over 20 inches, so there is abundant opportunities for EMI and signal attenuation.

It should be clear now that it is desirable to minimize stub lengths and the bus lengths of high-speed busses. Figure 3 shows a new bus topology that minimizes stub lengths and the total bus length for a high-speed expandable bus system. A similar main memory computing system is shown in this example, with a controller at one end of the bus and a termination resistor at the opposite end of the bus. In this topology, the bus system is looped in and out of the memory module, but the second port of the module bus is located at a different connector. By utilizing a second connection point, the bus can be routed vertically on the short module as opposed to the longer horizontal direction. In this approach, the continuation of the bus is maintained by a jumper from one module to the next, or one the motherboard itself, depending upon the module location. In the previous example, the bus is always continued on the motherboard.

The bus jumper can consist of two connectors for attaching to the DIMM PCBs, and a small section of PCB connecting the connectors, as depicted in Figure 4. There are many possibilities for implementing the jumper that do not effect the applicability of the invention. The connection point does not need to be at the top of the card, rather it can be located at some intermediate point on the card that would provide a distance advantage over looping the bus back to the connector it entered on. The jumper could also consist of flexible cable or coaxial cable, and the actual choice of mechanical or electrical connection can be established based on cost and desired data rates of the particular application. In the high-speed system, it would typically be desirable to match the impedance of the jumper to the impedance of the rest of the bus. In any scheme, the goal would be to provide two connection points on the module that offer the shortest possible bus distance.

This new bus topology and the topology shown in Figure 2 both require a routed card in every slot to maintain a continuous bus. If there is no active card in the slot, a routing card must be inserted in its place. A bus jumper may also be necessary for the unpopulated slot. This topology supports an even number of slots easily, but an odd number of slots can be supported by providing a bus jumper that connects the second connector on the odd module to the motherboard PCB.

The new bus topology clearly reduces bus stubs and minimizes the bus length, which addresses many of the concerns for long busses that were previously mentioned. This topology thereby provides improvements in bandwidth and EMI compared to the prior art. However, there are other more subtle advantages of this topology. In the prior art example of Figure 2, the number of bus signals (bus width) is must be practically reduced due to physical limitations of the connector and the routing congestion of the bus along the width of the module. Since there are two connection points for the new topology, the bus can contain more signals, because the same connector does not have to be used for the bus exit point. Further, routing the bus vertically reduces bus congestion for the example of a short, wide memory DIMM, since there is more space available in the width direction.

For a fixed number of memory devices on the bus, this topology would favor having a wider bus with fewer devices attached to each signal than the bus in Figure 2. This approach results in less devices per signal, and therefore, less capacitance per signal. This lower capacitance will allow the bus to operate at higher frequencies. Further, since there is fewer devices attached to a signal on the module, the populated section of the module will have less capacitance per unit length and a higher loaded impedance. The higher loaded impedance will allow a larger termination resistor to be use which will decrease the power dissipation of the bus for a given voltage swing. Additionally, the higher loaded impedance will allow narrow bus trace widths to be used in the unpopulated bus sections, and a uniform impedance can still be maintained. For example, the loaded impedance of the line may now approach 40 ohms in this case as opposed to 25-30 ohms in the previous example.

This invention has many possible applications and implementations that would not change the scope of the invention. These derivatives include, but are not limited to:

Main memory subsystems
Graphic cards
Input/Output cards
Peripheral cards
Network cards
Network hubs or switches
Bus jumpers implemented as:
- A PCB with connectors
- Flexible cable
- Permanent bus attachments instead of removable
- Coaxial lines
- Microstrip, stripline, or co-planar routing
- Reference planes used to maintain a uniform impedance
- Shield lines used to maintain a uniform impedance or reduce signal crosstalk
- Connections for signals only and not power and grounds
- Connections for signals and voltage references
- Bus connections in addition to unrelated signal connections for the purpose of module-to-module communication.
- The use of a reference plane on the jumper to reduce EMI

Connection points at the top and bottom of the card
Connection points at two sides of the card
Connection points at intermediate points on the card
Connectors other than DIMM connectors
Surface mount or through-hole connectors.

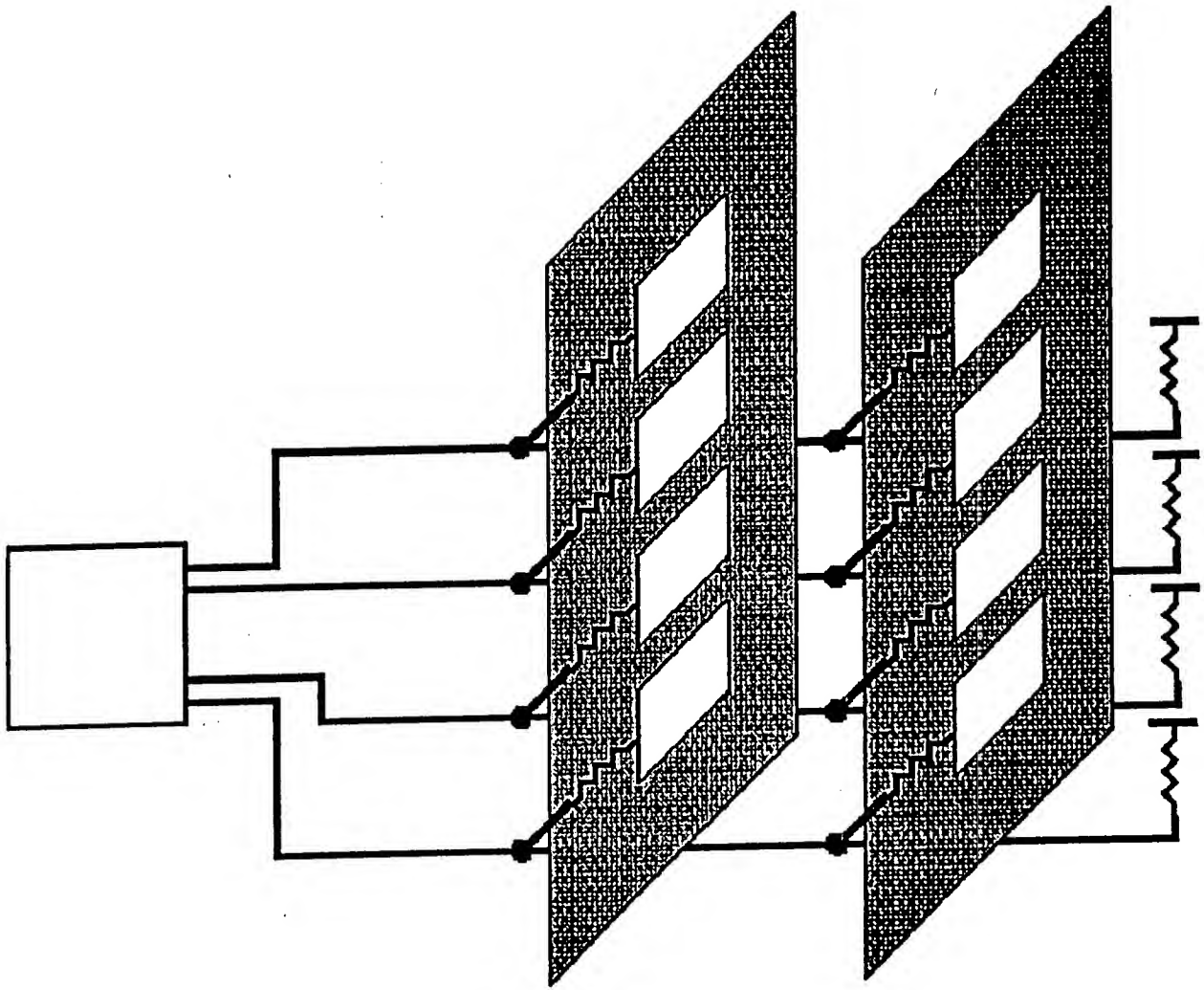
Many implementations are possible by those skilled in the art without changing the scope or intent of the invention.

Bus Topology Considerations

Terry Lee
tlee@micron.com

MSDRAM

Stub Bus Topology



HSDRAM

Stub Bus

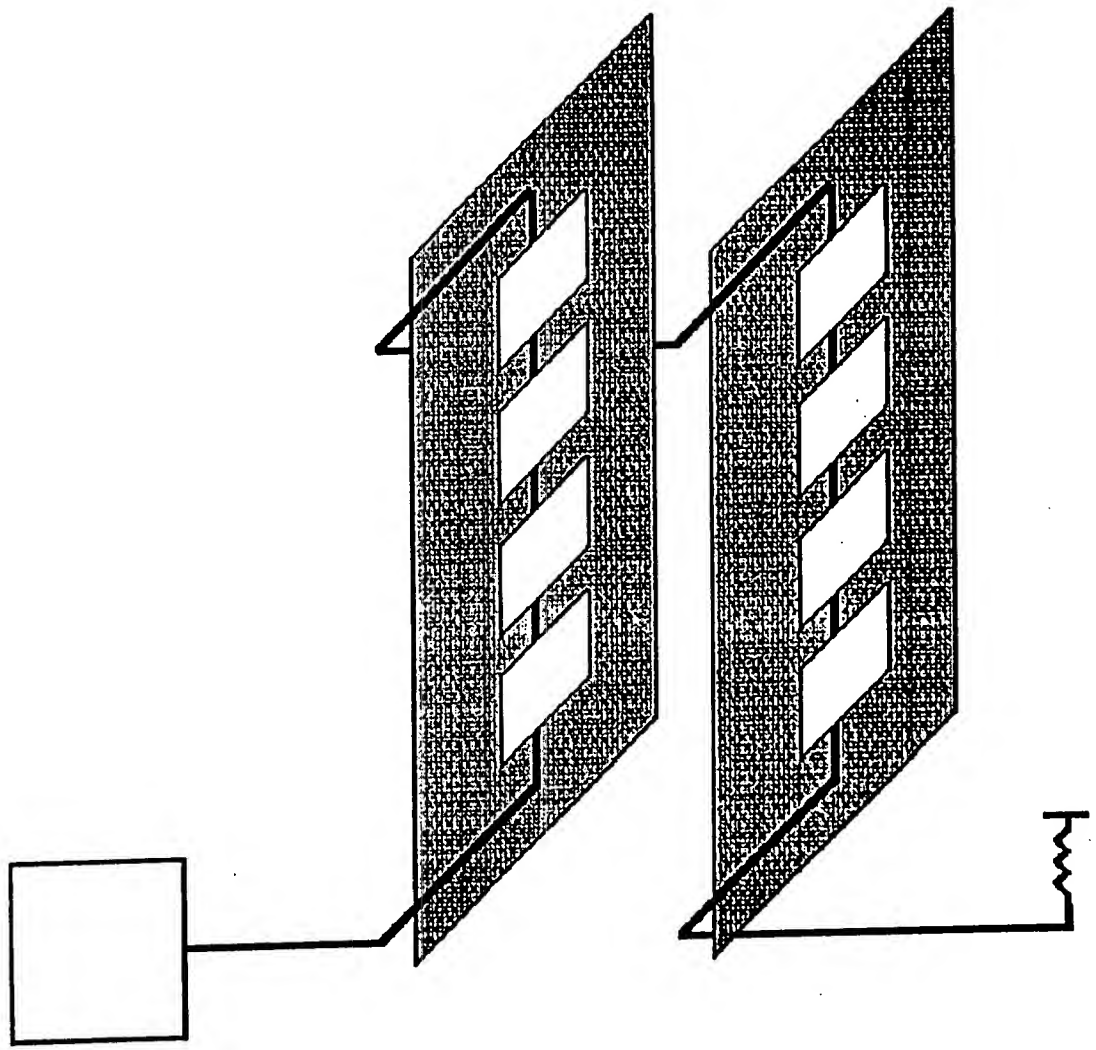
Advantages:

- Shorter bus length
  - Lower EMI
  - Shorter flight times
  - Less problems with symbol interference on bus turn-arounds
- No continuity module required
- Higher impedance connector is okay

Disadvantages:

- Stub resistor required even with shorter stublengths
  - Higher VDDQ required
- Difficult to match bus impedance in both directions (READs and WRITEs)
- Reflections must be managed

Loop-through Bus Topology



HSDRAM

Loop-through Bus

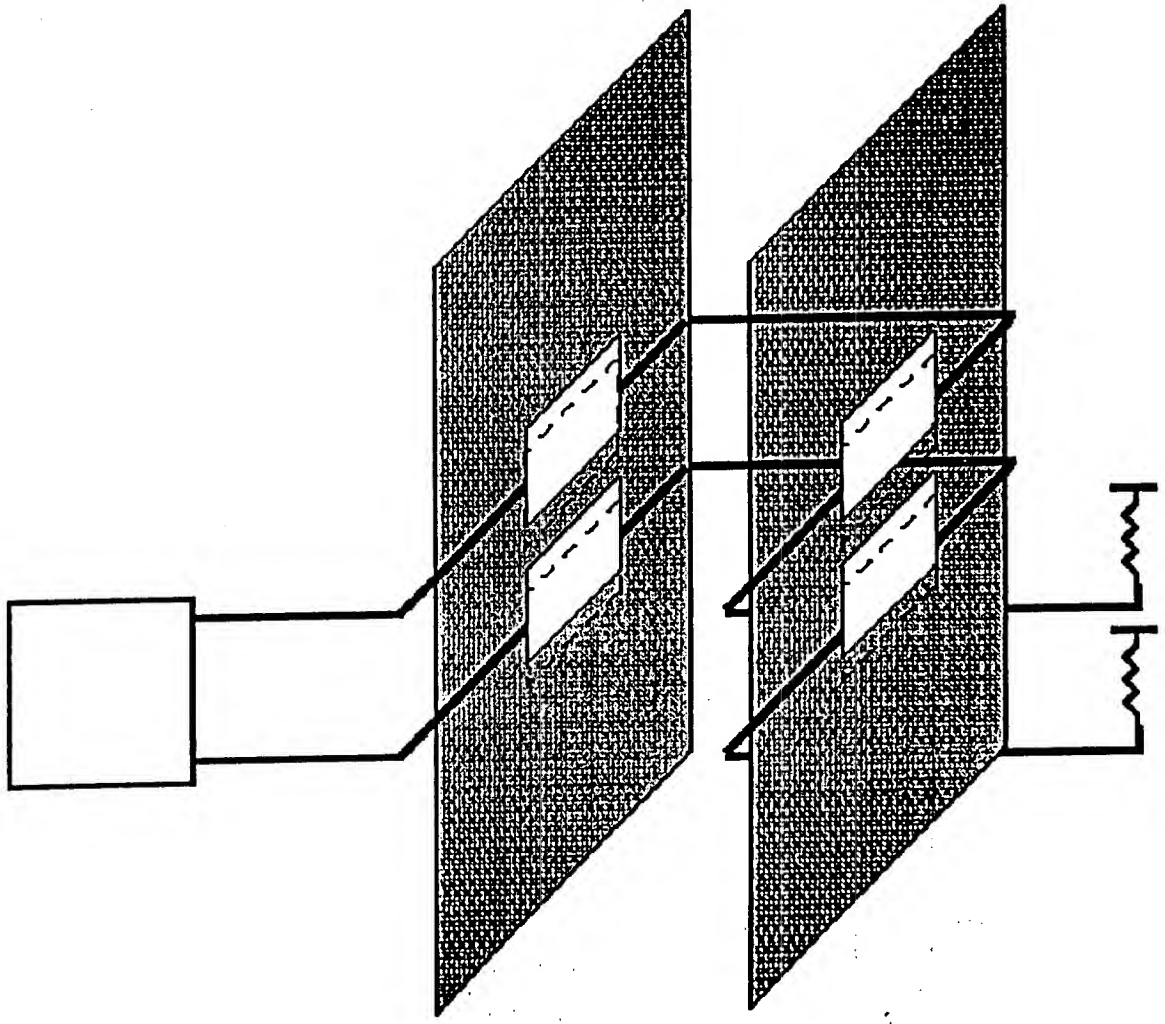
Advantages:

- Relatively constant channel impedance in both directions
  - Relatively small reflected energy
- No stub resistor required
  - Potentially lower VDDQ
- Higher potential bandwidth due to lower reflected energy

Disadvantages:

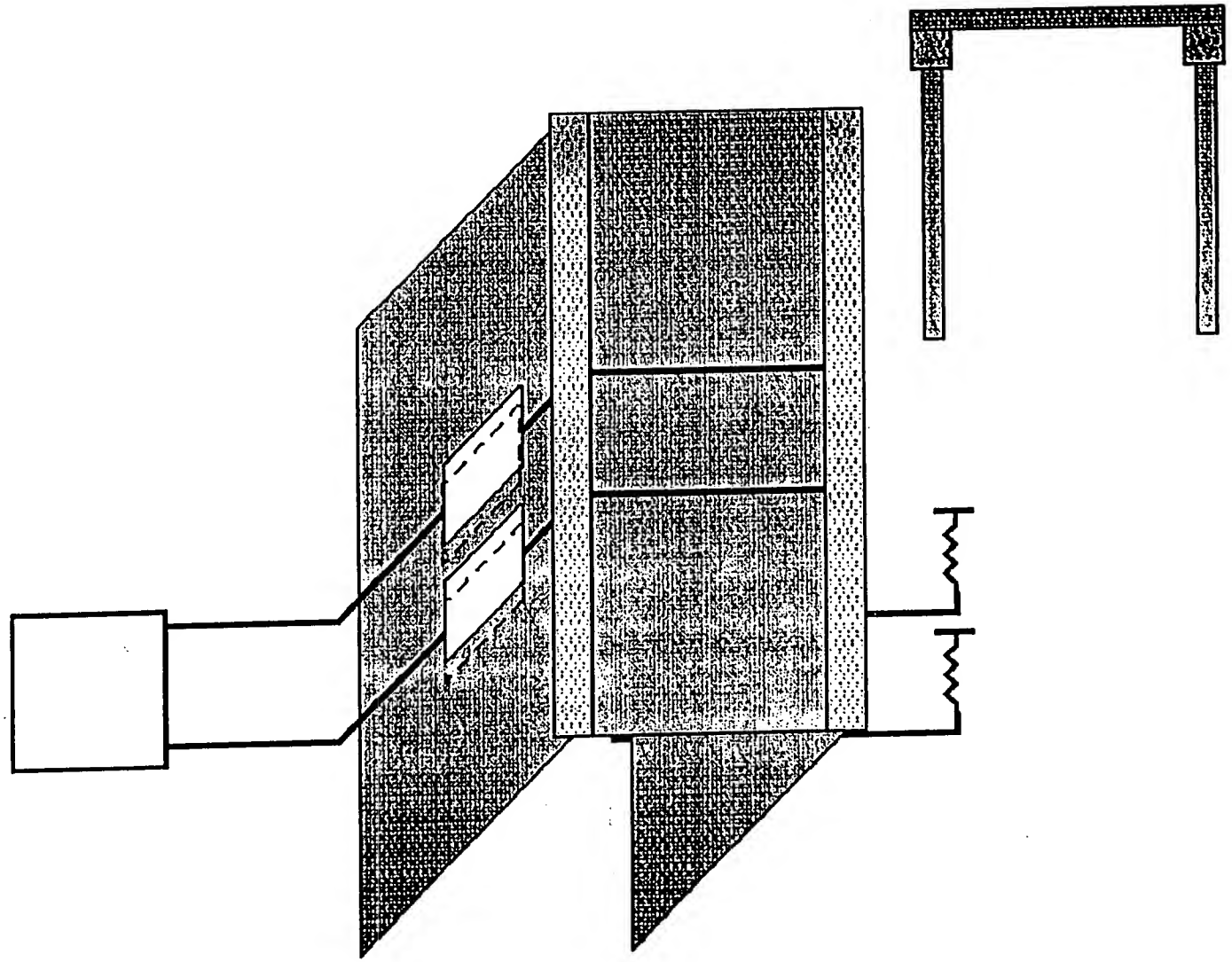
- Long bus length
  - Higher EMI
  - Long flight times
  - Symbol interference on bus-turnarounds
- Continuity modules required
- Assumes more devices loading per pin due to narrower bus
  - Relatively low loaded channel impedance results
- (4) connector interfaces in a (2) DIMM system

Proposed Short Loop Bus Topology



HSDRAM

DIMM-to-DIMM Interface



HSDRAM

Short Loop Bus

Advantages:

- All of the loop-through bus advantages plus:
- Shorter bus results in
  - Better EMI
  - Higher potential bandwidth
  - Less symbol interference problems
- Assumes wider bus and higher loaded channel impedance than loop-through bus

Disadvantages:

- Disadvantages of the loop-through bus, but shorter bus improves
  - EMI
  - Flight times
  - Symbol interference on bus turn-arounds
- Must add two connectors or interface connection
  - Still has the same number of connector interfaces though

HSDRAM

ASSIGNMENT AND AGREEMENT

For value received, I, Terry R. Lee hereby sell, assign and transfer to Micron Technology, Inc., a corporation of the State of Delaware, having an office at 8000 S. Federal Way, Boise, Idaho 83706-9632, U.S.A., and its successors, assigns and legal representatives, the entire right, title and interest, for the United States of America, in and to certain inventions related to an invention entitled HIGH SPEED BUS TOPOLOGY FOR EXPANDABLE SYSTEMS, described in an application for Letters Patent of the United States, which was filed on May 31, 2000, as United States Application No. 09/583,883, all the rights and privileges in said application and under any and all Letters Patent that may be granted in the United States for said inventions; and I also concurrently hereby sell, assign and transfer to Micron Technology, Inc. the entire right, title and interest in and to said inventions for all countries foreign to the United States, including all rights of priority arising from the application aforesaid, and all the rights and privileges under any and all forms of protection, including Letters Patent, that may be granted in said countries foreign to the United States for said inventions.

I authorize Micron Technology, Inc. to make application for such protection in its own name and maintain such protection in any and all countries foreign to the United States, and to invoke and claim for any application for patent or other form of protection for said inventions, without further authorization from me, any and all benefits, including the right of priority provided by any and all treaties, conventions, or agreements.

I hereby consent that a copy of this assignment shall be deemed a full legal and formal equivalent of any document which may be required in any country in proof of the right of Micron Technology, Inc. to apply for patent or other form of protection for said inventions and to claim the aforesaid benefit of the right of priority.

I request that any and all patents for said inventions be issued to Micron Technology, Inc. in the United States and in all countries foreign to the United States, or to such nominees as Micron Technology, Inc. may designate.

I agree that, when requested, I shall, without charge to Micron Technology, Inc. but at its expense, sign all papers, and do all acts which may be necessary, desirable or convenient in connection with said applications, patents, or other forms of protection.

Terry R. Lee

Date: 9-14-00

United States of America)
State of Idaho)ss.:
County of Ada)

On this 14th day of September, 2000, before me personally came Terry R. Lee, to me known to be the individual described in and who executed the foregoing instrument, and acknowledged execution of the same.

TRISH HOMAN-HAIDER NOTARY PUBLIC STATE OF IDAHO

Trish Homan-Haider
Notary Public
My Commission expires
3-26-03

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW • Washington, DC 20037-1526
Tel (202) 785-9700 • Fax (202) 887-0689
Writer's Direct Dial: (202) 828-2232
E-Mail Address: DAmicoT@dsmo.com

[redacted]

VIA FEDEX

Ms. Peggy Loyd-Fuster
Patent Assistant
Micron Technology
8000 S. Federal Way
Boise, ID 83707-0006

PRIVILEGED AND CONFIDENTIAL:
ATTORNEY-CLIENT COMMUNICATION

Re: Proposed U.S. Patent Application
Title: High Speed Bus Topology For Expandable Systems
Inventor: Terry R. Lee
Your Reference: 99-1184
Our Reference: M4065.0260/P260

Dear Ms. Loyd-Fuster:

Enclosed please find three copies of a first draft of a patent application for Micron's invention entitled "High Speed Bus Topology For Expandable Systems." This draft has been prepared based upon the original invention submission and a subsequent telephone interview with Mr. Lee. Please have Mr. Lee review this draft to ensure that it completely and accurately describes the invention.

Please direct any comments on the draft to Gianni Minutoli at (202) 861-9191 or his e-mail address is MinutoliG@dsmo.com. I trust you will be able to provide any comments within the next ten (10) days, so we can revise the application and get it filed as soon as possible.

If you have any questions, please do not hesitate to call.

Very truly yours,

Thomas J. D'Amico

TJD/GM
Enclosures (3 copies of application and figures)

Minutoli, Gianni

From: D'Amico, Thomas
Sent: [redacted]
To: Minutoli, Gianni
Subject: FW: Edits to 99-1184, High Speed Bus Topology for Expandable Syst ems

[redacted]

Thomas J. D'Amico, Esq.
Dickstein Shapiro Morin & Oshinsky, LLP
2101 L Street, N.W.
Washington, D.C. 20037
(202)-828-2232
(202)-887-0689 (fax)
[email to:DamicoT@dsmo.com]

-----Original Message-----
From: laboyer [mailto:laboyer@micron.com]
Sent: [redacted]
To: 'Tom'
Subject: FW: Edits to 99-1184, High Speed Bus Topology for Expandable Syst ems

-----Original Message-----
From: tlee
Sent: [redacted]
To: paloyd
Cc: laboyer; tlee
Subject: Edits to 99-1184, High Speed Bus Topology for Expandable Systems

Peggy,

Please pass these edits on to the patent attorney. Thanks.

Terry

P2, L20 - Please remove "or stub up"

P3, L6 - typo on resistor

P3, L15 - replace "is a 16-bit" with "may be a 16-bit"

P4, L11 - remove the last sentance of the paragraph

P6, L16 - add "voltage swing" after signal.

P8, L15 - replace "maximum" with "greater"

P8, L21 - replace "maximum" with "greater"

P9, after L12 - I might need to add an another implementation, but we should discuss this to determine if can be claimed. The added language would read "In another implementation, the bus is routed vertically from one pin of the connector to the devices, and then returns through a short path to a different connector pin. In one implementation, the input pin and output pin of the bus may be on separate sides of the connector." If we agree that this can be claimed, then it would have several impacts throughout the document. The first place I noticed an impact was on P9, L4. We need to look at some prior art to determine whether this would be allowed.

P10, after L11 - If the forementioned implementation is allowed, we would need to add a Figure 10. "Figure 10 is a diagram illustrating another embodiment of the present invention where the bus enters and exits different pins of the connector through a short path."

P11, L14 - after respectively ", or at some intermediate portion of the cards, or the bottom of the cards on the same connector." The second half of this addition is subject to allowance.

P12, L16 - before Bus portions. "In another embodiment of the present invention, the bus can route out of the same connector on a different pin, such as a pin on the opposite side of the connector, with a short path length."

P13, L16 - Just a question. Could we claim the invention where the bus is routed through the module in a predominantly vertical fashion to minimize the bus length? The routing could come out the top or back down through the same connector. This would be different than the RIMM routing, depending upon claims.

P14, L3 - change "size" to "impedance".

P22 - claims would needed to be added for the up/down bus, if allowed.

P25, L22 - replace "out of the second slot" with "near either or both ends of the bus"

P27, after L11 - New claim dependent claim 27a. The method of claim 14 wherein only a portion of the signals are routed between the first and second cards, and other signals route into the card by connections to the motherboard only.

P30, after L5 - New dependent claims. 38a - The system of claim 37 wherein said cable is a ribbon cable with a shield. 38b - The system of claim 37 wherein said cable is a coaxial cable. 38c - The system of claim 37 wherein said cable is twisted pair wiring. 38d - The system of claim 37 wherein said cable is a waveguide.

P32, afer L14 - New dependent claims. Add 48a, b, c, d as per 38a,b,c,d.

P33, L22 - Question. Does "coupled to said processor" include the case where the processor is connected to a memory controller (a separate chip),

and the memory controller connects to the memory bus system? This is a typical scenario. We need to cover this configuration as well.

Possible additions to the claims:

Is the case where >4 slots covered?

There could be some memory devices soldered down on the motherboard that are connected to the bus, in addition to the devices on the modules. Do we need to add claims to cover this?

Another key application to mention besides the computer, is a networking hub, switch, or router.

This bus can be extended by adding a repeater chip (transmit/receive re-driver) at the end of the bus to drive a second bus (extension of the first). Would we need to claim this?

It is advantageous for the memory devices to use a high dynamic impedance driver (such as a saturated, open-drain type) to drive this type of bus. Does this need to be added as a dependent claim?

This bus structure could also be used to transport a non-digital signal, such as RF modulated information, where the digital information is encoded on an analog waveform. Does this need to be added as a dependent claim?

The biggest outstanding issue is regarding allowing claims for the up/down bus. We should discuss this. Otherwise, I think we are very close on this disclosure. Please use change bars on the next revision, and I can just review the changes, and we can file. Thanks.

Terry Lee

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW • Washington, DC 20037-1526
Tel (202) 785-9700 • Fax (202) 887-0689
Writer's Direct Dial: (202) 828-2232
E-Mail Address: DAmicoT@dsmo.com

[redacted]

VIA FEDEX

Ms. Lisa A. Boyer
Patent Assistant
Micron Technology
8000 S. Federal Way
Boise, ID 83707-0006

PRIVILEGED AND CONFIDENTIAL:
ATTORNEY-CLIENT COMMUNICATION

Re: Proposed U.S. Patent Application
Title: High Speed Bus Topology For Expandable Systems
Inventor: Terry R. Lee
Your Reference: 99-1184
Our Reference: M4065.0260/P260

Dear Lisa:

Enclosed are three copies of a signature draft of the patent application for Micron's invention entitled "High Speed Bus Topology For Expandable Systems." The draft includes all of the revisions requested by Mr. Lee. Per Mr. Lee's request, we are also providing a single red-lined version of the application.

Please have Mr. Lee review this signature draft one more time for accuracy and completeness. If in the final review you note the need for any minor revisions, please call and we will discuss how to handle those. Also enclosed are the Declaration for Patent Application, Assignment and Agreement, and Power of Attorney by Assignee and Certificate by Assignee Under 37 C.F.R. § 3.73(b) forms. Please have the application executed and returned to us at your earliest convenience. We will file it as soon as we receive it.

If you have any questions, please do not hesitate to call.

Very truly yours,

Thomas J. D'Amico

TJD/GM
Enclosures (3 copies of application and figures, 1 copy of red-lined application for inventor Lee)

1177 Avenue of the Americas • 41st Floor • New York, New York 10036-2714
Tel (212) 835-1400 • Fax (212) 997-9880
http://www.dsmo.com

Minutoli, Gianni

From: D'Amico, Thomas
Sent: Tuesday, May 30, 2000 10:55 AM
To: [redacted]; Minutoli, Gianni
Subject: FW:

Thomas J. D'Amico, Esq.
Dickstein Shapiro Morin & Oshinsky, LLP
2101 L Street, N.W.
Washington, D.C. 20037
(202)-828-2232
(202)-887-0689 (fax)
[email to:DamicoT@dsmo.com]

-----Original Message-----
From: laboyer [mailto:laboyer@micron.com]
Sent: Tuesday, May 30, 2000 10:46 AM
To: 'Tom'
Subject:

Here are some changes from Terry Lee

-----Original Message-----
From: tlee
Sent: Friday, May 26, 2000 11:39 AM
To: laboyer
Cc: tlee
Subject:

Lisa,

Please forward this information to the appropriate people. Thanks.

Terry

99-1184 (High Speed Bus Topology for Expandable Systems)

File as is.